SYSTEM AND METHOD FOR CHIP TESTING

ABSTRACT OF THE DISCLOSURE

A system and method for chip testing is disclosed. The present invention's method includes the steps of establishing a communications link between a chip and a computer tester; receiving on the chip an initial test algorithm over a communications link; testing the chip, using a built-in self-test (BIST) circuit on the chip, in accordance with the initial algorithm; collecting a set of failure information in response to testing; and transmitting the failure information from the chip to the computer over the communications link. The present invention's system includes: a communications link; a computer, operating a set of chip testing software; and a chip under test coupled to the computer by the communications link, having, a memory array; and a BIST module for testing the memory array in response to test algorithms received from the computer and transmitting those addresses within the memory array which failed testing.